AMENDMENTS TO THE CLAIMS:

1-40. (Canceled).

41. (Currently Amended) A multi-chip module package structure comprising:

a multi-chip module substrate;

at least two chip packages, each of said chip packages being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least two chip packages having been burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said chip packages with said multi-chip module substrate;

a plurality of electrical connect pins; and

a package material enclosing said multi-chip module substrate, said connect points and said chip packages;

wherein said multi-chip module package structure is a ball grid array package.

42. (Previously Added) The multi-chip module package structure as claimed in claim 41, wherein each of said chip packages is a chip-scale package or a wafer level chip-scale package.

43. (Previously Added) The multi-chip module package structure as claimed in claim 41, wherein at least one of said chip packages is a chip-scale package with wire bonding.

44. (Previously Added) The multi-chip module package structure as claimed in claim 41, wherein at least one of said chip packages is a chip-scale package with flip chip

bonding.

45. (Previously Added) The multi-chip module package structure as claimed in claim 41, wherein at least one of said chip packages is a chip-scale package with central pad bonding.

46. (Canceled).

47. (Previously Added) The multi-chip module package structure as claimed in claim 41, wherein said plurality of electrical connect pins are solder balls.

48. (Previously Added) The multi-chip module package structure as claimed in claim 41, wherein said plurality of electrical connect points are solder balls or gold wires.

49. (Currently Amended) A multi-chip module package structure comprising:

a multi-chip module substrate;

at least a bare chip;

at least one chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least one chip package having been burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said bare chip and said at least one chip package with said multi-chip module substrate;

a plurality of electrical connect pins; and

a package material enclosing said multi-chip module substrate, said connect points, said bare chip and said at least one chip package;

wherein said multi-chip module package structure is a ball grid array package.

50. (Currently Amended) The multi-chip module package structure as claimed in claim 49, wherein said bare chip is bonded to said multi-chip module substrate by wire bonding or flip chip bonding.

51. (Previously Added) The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package or a wafer level chip-scale package.

52. (Previously Added) The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package with wire bonding.

53. (Previously Added) The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package with flip chip bonding.

54. (Previously Added) The multi-chip module package structure as claimed in claim 49, wherein said at least one chip package is a chip-scale package with central pad bonding.

55. (Canceled).

56. (Previously Added) The multi-chip module package structure as claimed in claim 49, wherein said plurality of electrical connect pins are solder balls.

57. (Previously Added) The multi-chip module package structure as claimed in claim 49, wherein said plurality of electrical connect points are solder balls or gold wires.